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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/259,145	02/26/1999	PAI-HUNG PAN	3027.1US	4919

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EXAMINER
MAI, ANH D

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/259,145	PAN ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25,26,31-34,37-40 and 43-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25,26,31-34,37-40 and 43-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The amendment filed November 28, 2000 (and again in October 15, 2001) is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure, "*a semiconductor substrate free of field oxide structures*", as previously applied.

2. Claims 25, 26, 31-34, 37-40 and 43-49 are rejected under 35 U.S.C. 112, first paragraph, for containing subject matter which was not described in the **specification** in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention, as previously applied.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 11, 2002 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 25, 26, 31, 33, 34, 37-40 and 43-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tada (U.S. Patent No. 5,545,577) in view of Koike (5,874,325).

With respect to claims 25, 33, 39 and 46, as best understood by the examiner, Tada teaches an intermediate structure in the formation of an isolation structure for a semiconductor device substantially as claimed including:

a semiconductor substrate (100) free of field oxide structures and having a first surface and a second surface, the first surface opposing the second surface;

at least one p-well (3) and at least one n-well (2) on the substrate first surface;

at least one activated, annealed p-type area (5) within the at least one n-well (2);

at least one activated, annealed n-type area (6) within the at least one p-well (3); and

a substantially dopant-free, uninterrupted diffusion barrier layer over the substrate first surface. (See Fig. 2c and 3a, col. 6, ll. 3-32).

Thus, Tada is shown to teach all of the features of the claim with the exception of the substantially dopant-free barrier layer is formed encapsulating the semiconductor substrate.

However, Koike teaches a substantially dopant-free barrier layer (104) is formed on the first surface, consequently formed on the second surface thus, encapsulating the semiconductor substrate (101).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the substantially dopant-free barrier layer of Tada on the first surface of the semiconductor substrate (100) as taught by Koike to encapsulating the semiconductor substrate to prevent the second surface from oxidizing.

Further, intermediate semiconductor substrate of Tada appears to be free of field oxide structures. (See Fig. 2c).

Note that, the p-type area (5) and n-type area (6) of Tada ***are formed*** in the wells (2,3), thus, activated. Moreover, to activate the dopants, the substrate must be annealed. (See S. Wolf et al., Silicon Processing for the VLSI Era)

With respect to claims 26, 34, 40 and 47, the structure of Tada also includes an oxide layer (4) between the substrate first surface and the substantially dopant-free barrier layer.

With respect to claims 31, 37, 43 and 48, the substantially dopant-free barrier layer of Tada is silicon nitride.

With respect to claim 38, the at least one activated, annealed doped area of Tada comprises an impurity selected form the group consisting of a n-type impurity and a p-type impurity.

With respect to claim 44, the at least one activated, annealed first doped area of Tada comprises a p-type impurity (2) and the at least one activated, annealed second, differently doped area comprises an n-type impurity.

With respect to claim 45, the at least one activated, annealed first doped area of Tada comprises an n-type impurity (2) and the at least one activated, annealed second, differently doped area comprises a p-type impurity.

3. Claims 32 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tada '577 and Koike '325 as applied to claims 25 and 46 above, and further in view of Shim et al. (U.S. Patent No. 5,846,596).

Tada and Koike teach all of the features of the claim with the exception of using silicon oxynitride for the substantially dopant-free barrier layer.

However, Shim teaches the oxidation resistant layer (130) comprising silicon oxynitride (130). (See col. 3, ll.18-20).

It would have been obvious to one having ordinary skill in the art at the time of the invention to form the substantially dopant-free, uninterrupted diffusion barrier layer of Tada using silicon oxynitride as taught by Shim because it has an added advantage of oxidation resistance.

Response to Arguments

35 U.S.C. 132 Objection and 112, first paragraph:

Applicant's arguments filed February 11, 2002, regarding 35 U.S.C. 132; 112/ first paragraph, have been fully considered but they are not persuasive.

Applicant appears to rely on the drawings to support his contention that the semiconductor substrate is free of field oxide. However, the drawings are not drawn to scale. (MPEP 2125). Thus, the drawings by themselves can not be relied upon to claim the subject matters that are not disclosed. There are many things that are inherent of the intermediate structure. However, "semiconductor substrate free of field oxide" is not one of them.

Furthermore, the specification on page 7, paragraph 1 indicates that "[I]t should be understood that the figures presented in conjunction with this description ***are not meant to be actual cross-section views*** of any particular portion of an actual semiconductor device, but ***are merely idealized representations*** which are employed to more clearly and fully depict the process of the invention than would be otherwise be possible".

Thus, M.P.E.P 2163.06 only allows for the subject matters that are disclosed.

Applicant presently states, "[S]ince these field oxide structures are grown on the semiconductor substrate after the intermediate structure is annealed, the field oxide structures are necessarily not present on the semiconductor substrate until after the intermediate structure in annealed". However, the specification on page 2, lines 10-12 states: "[F]or the shake of example only, the follow discussion *will focus on* the formation of a twin-well CMOS (Complementary Metal Oxide Semiconductor) structure". Which clearly means that there are some devices may be already formed somewhere else on the semiconductor substrate. Therefore, the specification, as originally filed, **does not explicitly or implicitly support** the Applicant's contention that the semiconductor substrate is "free of field oxide structures".

Applicant further state that drawing also provide support for the term "free of field oxide structures" because they show the "intermediate structure" before and after the anneal.

At best, the drawings can be interpreted as: "a semiconductor substrate, **at the CMOS region**, free of field oxide structures", because the drawings **only** illustrate the absence of field oxide structures at the CMOS region, not the semiconductor substrate as a whole.

The objection and the rejection under 35 U.S.C. 132 and 112, first paragraph, regarding the limitation "a semiconductor substrate free of field oxide structures" are therefore, maintained.

Rejection under Tada '577 in view of Koike '325.

Applicant argues "[I]n contrast, Tada discloses a method of producing a semiconductor device that has two MIS transistor circuits on a first surface of the device".

First of all, the present claims do not preclude the existing of any device, any where.

Secondly, the Applicant fails to show where are the MIS transistor circuits in Fig. 2c.

Applicant further argues "[A] silicon nitride layer is used as a mask to form a field oxide film on the first surface of the semiconductor substrate".

This portion reads on the formation of the dopant-free, uninterrupted barrier layer of the claims. Because the instant silicon nitride layer 120 (dopant-free, uninterrupted barrier layer) is used as a mask to form a field oxide film 130 on the first surface of the semiconductor substrate 102. (See Figs. 3-7).

In response to applicant's arguments against the references individually such as Tada does not discloses that the barrier layer extends over the second surface of the substrate and Koike does not disclose p-well and n-well on the first surface of the substrate or activated, annealed n-type and p-type areas within the p-wells and n-wells, respectively, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The *prima facie* case of obviousness has been established because what Tada lacks, the barrier layer on the second surface, is provided by Koike and the motivation to combine has been given. Since the Applicant is silent on the motivation, one should conclude that the Applicant has agreed on the reasoning provided.

The similar is also applied to the arguments with respect to claims 33, 39 and 46.

Rejection under Tada '577 and Koike '325 and further in view of Shim '596.

With respect the selection of silicon oxynitride material (Shim) for the barrier layer. (Claims 32 and 49). Since Tada and Koike are shown to teach all the features of the claims (25 and 46), the selection of the material for the barrier layer is no more than a design choice. A motivation to combine is given and agreed upon by the Applicant.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references are cited to show the state of the art regarding:

-How the diffusion layers are formed. S. Wolf et al., *Silicon Processing*.

-Forming a layer over one surface will consequently formed over the other surface. JP-61-159741 and JP-05-109736.

5. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M

March 18, 2002

Olik Chaudhuri
Supervisory Patent Examiner
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